Solid State Devices

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Lecture - 42

The Final Lecture

Welcome to the final lecture of this course on Solid State Devices. I was wondering after discussing so much in the last 41 lectures on semi conductor devices what shall we do in this final lecture. At this point I am reminded of a program on All India Radio. This program is called Aap Ki Farmaish in Hindi or Ungal Viruppam in Tamil. Basically in this program the songs which are suggested by the listeners are played. So what it means is, it is the listener's choice, that is, your choice. So accordingly I think what I will do is that I will let you ask me questions on various aspects of semi conductor devices or semi conductors because there are so many devices existing that it is difficult to decide on which devices to cover in a course and all the devices cannot be covered in a course. Let us start today's class with a question and answer session. Here is the first question.

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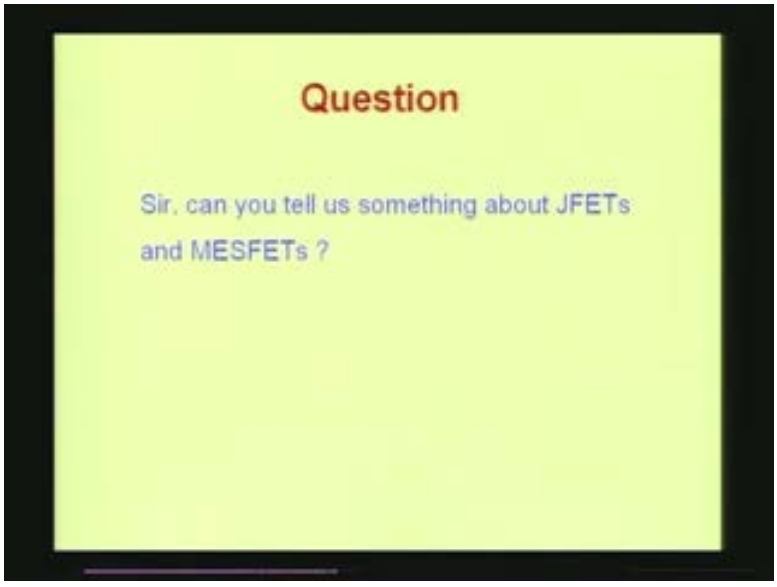

Sir, can you tell us something about JFETs and MESFETs?

Let us see what are the JFETs and MESFETs. Let us start with the JFET. The JFET is the Junction Field Effect Transistor.

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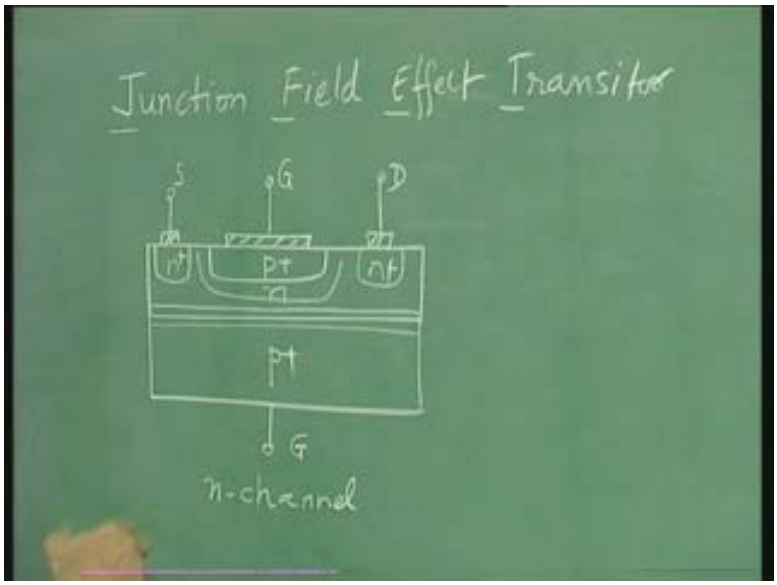

So it is JFET. What we will do is, we will consider the structure and processing and then the operation and application of this device. We will discuss all these aspects very briefly. Let us see the structure of the JFET. Basically you start with a heavily doped substrate p-type and on this you grow an epitaxial layer which is n-type and in this you diffuse a heavily doped p-type layer. This region between the two p + regions is a channel so what we are drawing here is an n channel JFET. The source and drain are on either sides of the device so here you have the source and here you have the drain which is also made by diffusion. So this is your gate, this substrate also acts like a gate. So normally this particular substrate and this diffusion the p + diffusion on the top are connected together to form a common gate. This is the source and here you have the drain.

Now, how does this device operate?

You see that this is the channel region which conducts between drain and source. When you apply a voltage to the drain with respect to source if the channel is open then it will conduct current.

Now how do you know that the channel is open and how do you control the width of the channel?

So it is a very simple PN junction theory which tells you that there is a depletion region here and this depletion region will vary as you change the voltage here at the gate. You have a depletion region from this p + side also. In fact we must show this depletion region on the p + side as very negligible because most of the depletion region will be on lightly doped side.

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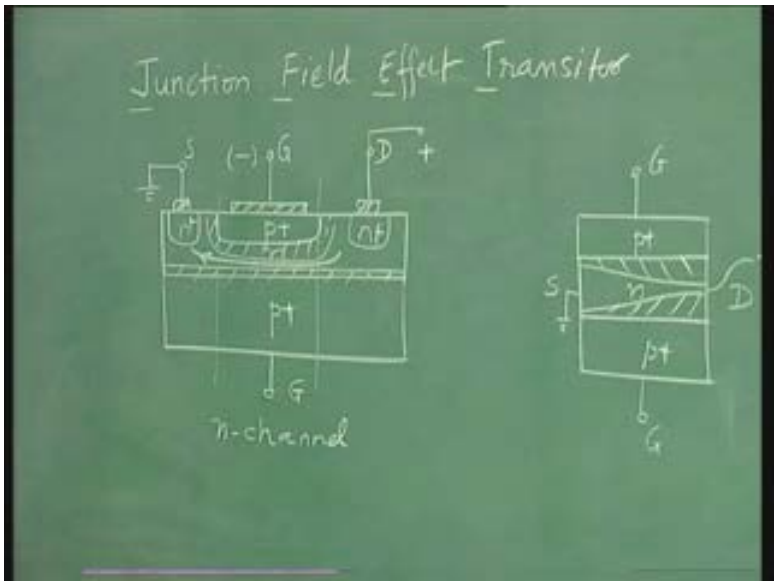

So this is a depletion region and this is a depletion region. We can see that when you vary the gate voltage these two depletion regions will vary. So, as you increase the gate voltage the channel which is this region through which the current can flow between drain and source gets modulated. And if the gate voltage is sufficiently large in the reverse direction, please note this is the PN junction so to deplete the channel you will need to apply a negative voltage. Even when the voltage is 0 you will have some depletion regions here so the channel will not be fully open.

You can apply a positive voltage to the gate to further reduce the depletion width over the equilibrium condition and open the channel. Please remember that you cannot apply a high forward bias because then the gate current will be large. You can apply a forward bias of about0.5V utmost here. But otherwise this device will mostly operate with the gate to channel

reverse biased so the polarities would be as follows. So you will ground the source and you will apply a positive voltage to the drain.

Now when you do that obviously the depletion region will not be uniform throughout the device it will be more at the drain and small at the source because the reverse bias between the channel and the gate is more near the drain as you can see the polarity from here, this is plus and this is minus whereas this is only 0. So, this reverse bias is less than this reverse bias. So, if you draw the depletion regions more carefully and what we do is we isolate only this particular region of the transistor for a simple analysis, it will look like this as follows:

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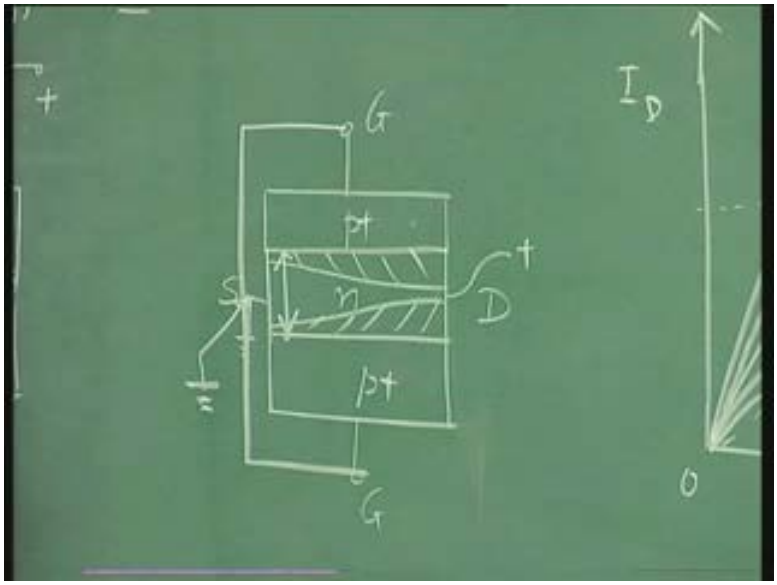

So this is the p + and this is the p + from the bottom, these are the gates, this is the channel. And now here you have the drain so your depletion region will vary like this and from here also it will vary like this. So, this is the source, this is the drain and this is the gate. So, as you go on increasing the drain voltage starting from 0 with respect to the source your current will increase but once these two depletion regions touch the current cannot change much as it happens in a MOSFET, so you have reached saturation. So, the characteristics of all the Field Effect Transistors have similar shapes.

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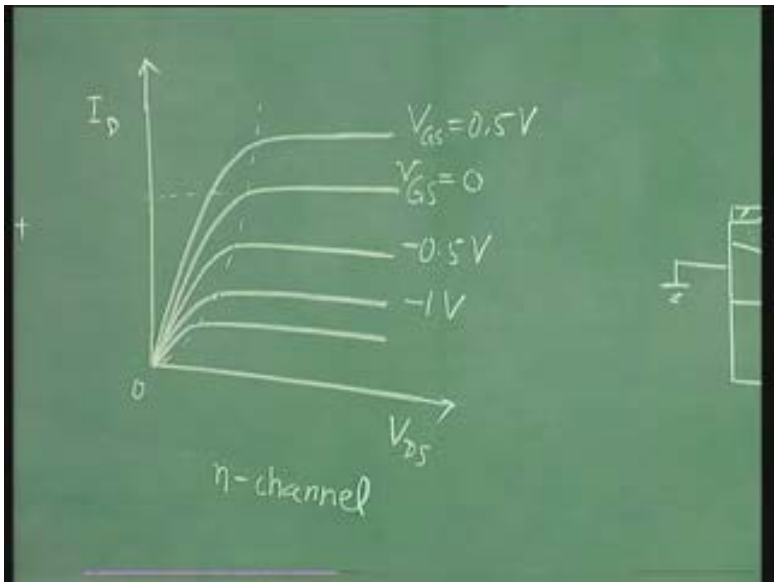

Therefore if I draw the characteristics for this device they would look as follows:
You have the so-called ohmic or linear region and saturation region and the currents are something like this so let us say this curve corresponds to VG = 0 VGS and this curve corresponds to VGS = 0 0.5 volts and as you go down you have the curves for more and more negative voltages. So this is ID versus VDS. These are the kind of characteristics you get.

Now, in the JFET you can have enhancement type device or a depletion type device like in any other Field Effect Transistor. In an enhancement type device what would happen is that the distance between this p + n junction and this p + n junction is so small, let us look at this diagram here that is the distance between these two. So this distance would be so small that even when you do not have a gate bias applied under equilibrium conditions the depletion regions form these two sides which will touch each other. Only when you apply a positive voltage to the gate or forward bias to the gate with respect to channel the channel will open. Therefore such a device would be called an enhancement type device.

Now these characteristics we have shown here correspond to a depletion type device because you can see that when no gate voltage is applied there is a large current and you can reduce the current. This is as far as the operation of the JFET is concerned.

What are the applications of this device?

The JFET is not a device which has very wide applications like the MOSFET. However, it is used in a few applications, the processing of this device is compatible with BJT so people do talk of a bi FET logic technology and bi FET means bipolar and JFET combined together to form logic gates, that is one of the applications. This JFET is also used as a current limiter even when you do not apply a gate to source voltage or rather the gate to source voltage is 0 that means you are shorting the gate to source which is something like this.

So, in this mode the device acts like a current limiter. You see, the maximum current cannot exceed this particular value. These are some of the applications. Now let us understand, what MESFET is which a device very similar to the JFET.

Now, before I discuss the MESFET let me tell you the fact that the JFET was the first practical Field Effect Transistor device that was made. You recall, we discussed the history of the Field Effect Transistor. The Field Effect Transistor, that is, the MOSFET concept was proposed in as early as 1925. But they could not realize MOSFET and in the process of trying to understand the difficulties they discovered the Bipolar Junction Transistor in 1948.

There after people were concentrating on the Bipolar Junction Transistor. And in fact this JFET was proposed by William Shockley in 1953 as a possible practically realizable Field Effect Transistor. So this is the first Field Effect Transistor that was made in practise the JFET in 1953. The advancement in the technology of this device however came in late 1970s only because 1950s was devoted to bipolar transistor, 1960s was devoted to MOSFET because around 1960 the integrate circuit was invented and there after the MOSFET was found to be very suitable for this integrate circuit. So in 1970s only the junction FET technology was developed. This device was applied in practise in many circuits.

Now let us come to the MESFET. This device was practically realized in 1966. The MESFET is a metal semiconductor FET. So it is Metal Semiconductor and FET Field Effect Transistor and that is how you get MESFET.

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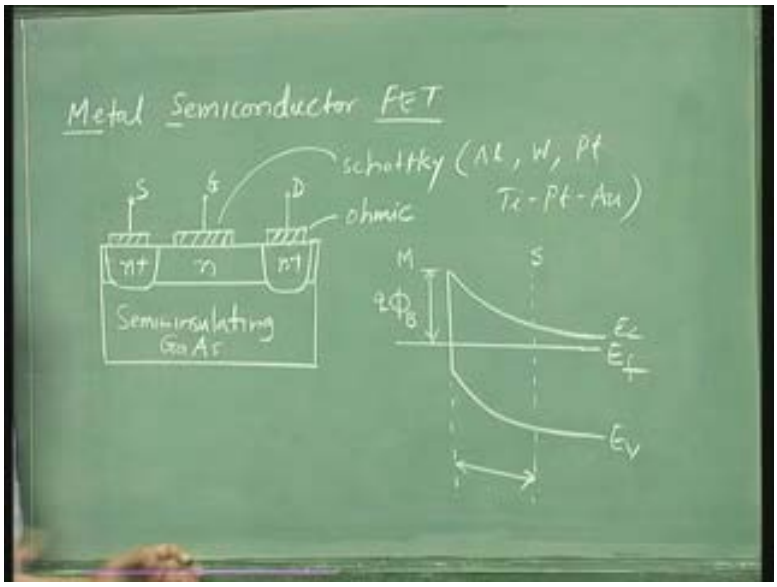

What is the structure of this device? The structure of this is device is very similar to the JFET. This device is generally made in compound semiconductors, so you start with a semi insulating gallium arsenide substrate. Then on this you epitaxially grow an n-type region. Please note that we are discussing an n channel device. In a JFET you can also get a p channel device if you interchange n and p-type regions. But in a MESFET generally only n channel devices are used. We will see why it is so.

On this particular epitaxial region you deposit a schottky type gate contact as a gate. And you also have source and drain contacts which are ohmic contacts. Underneath this region it is converted into a heavily doped region so that the ohmic contact is good. Let us say this is the source and here you have the drain and this is the gate. So this contact is schottky type whereas this is an ohmic contact. So, schottky type contact is one which has rectifying properties.

Now this is the structure of the MESFET. This structure appears simpler than the JFET because there are no PN junctions here as what you had found in a JFET. So this particular structure has processing advantages over the JFET. You do not have to do any high temperature diffusion to make the gate. Obviously whenever you have advantage you also have disadvantages. The disadvantage is that the built in voltage of this particular junction is not very high. So for the schottky junction the built in voltage is not very high.

Now what are the metals that are used to make the schottky type contact?
The metals used are: Aluminium, tungsten, platinum or titanium platinum gold a tri layer combination. This means that first you deposit titanium and on the top of that you will platinum and on the top of that you will have gold. These are the metals which are normally used to make schottky contact on gallium arsenide. The important thing to achieve here is that this particular schottky junction should have a good rectifying property. That means it should have very good barrier height.

What is barrier height?
You can draw the energy band diagram to understand this particular parameter. If you draw the energy band diagram of this particular schottky junction metal n-type semiconductor it would look as something like this. I am drawing it at 0 bias. This is the metal and this is the semiconductor. This is a n-type semiconductor so this Fermi-level is close to the conduction band edge and here you have the valance band edge in the bulk, and this is the so called depletion region. This difference is called the barrier height.

Now, this difference can be easily obtained from the work function of the metal and also the work function of the semiconductor. So you can draw the energy band diagram, I will leave this to you as an exercise to express phi B in terms of the work function of the metal, the electron affinity of the semiconductor and the Fermi-level difference between Ec and the Fermi-level location compared to Ec. So this height if it is large then you have a high built in potential, you have more band bending and therefore you have better rectifying properties and this is what you need to achieve in a MESFET.

Now what about the operation of this device?
Well, exactly like the JFET. Please look at this particular structure of the JFET we have discussed here. All that you need to do is replace this p + region by a metal and you have a similar depletion region except that the bottom is not another metal instead of this you have a semi insulating substrate. So this depletion region would not be present in a MESFET. In a MESFET your picture would look something like this.

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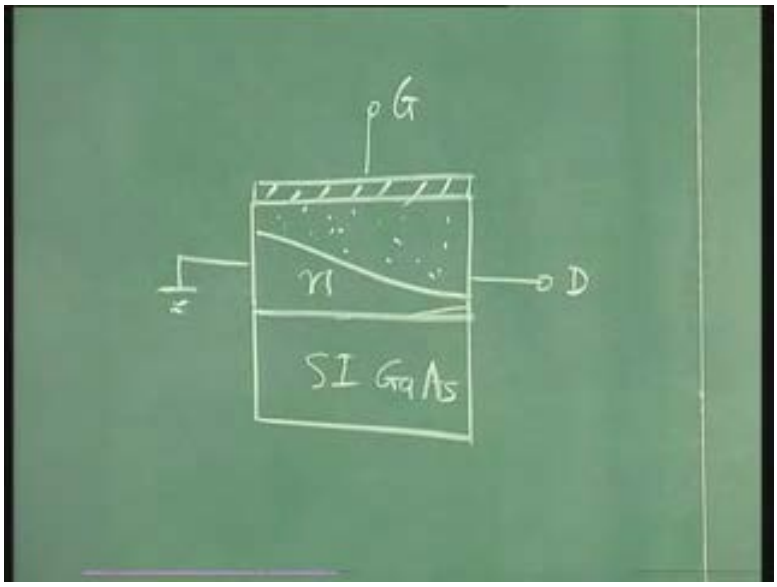

This is your metal schottky contact and this is the semi insulating gallium arsenide, SI stand for semi insulating and here you have the depletion region something like this. This depletion region is really very small because if it is semi insulating most of the depletion region would be in the substrate.

So this is the depletion region here. This is source, this is the drain and this will be the gate. Now, like the JFET you can have enhancement type and depletion type MESFETs.

What are the applications of this device?
This device has wide application in microwave range. So it is used as a power amplifier or as a switch or even for purposes like making oscillators generating frequencies. So, microwave range meaning you have applications of this device in the order of tens of gigahertz. Let us see one difference between MESFET and JFET.

If you look at the characteristics the disadvantage of the MESFET is that you cannot go up to a forward bias of 0.5 volts. Please note that these are characteristics for n channel device. In a MESFET you would probably be able to go up to 0.2 volts and that is the limitation of the MESFET.

So, in an enhancement type MESFET you cannot have a very wide voltage swing. This is the main difference between JFET and MESFET that is in terms of the disadvantage of the MESFET. But the advantage as we have said is easy to process. And this device is generally made in compound semiconductors which provide high mobility in the channel for the electrons and also because it is made on a semi insulating substrate the depletion region is very wide in the substrate and from PN junction theory you know that if the depletion region is wide the capacitance is very small. This combination of high mobility and the low capacitance enables you to go up to very high frequencies and that is why this device is used for microwave applications.

Now, one point I was mentioning is that you do not have p channel MESFETs. The reason is it is very difficult to find or make rectifying schottky contacts on p-type semiconductors. Unlike in a JFET where you can have p + n junction or n + p junction in a MESFET the schottky contact has a good barrier height and rectifying properties only if it is made on a n-type semiconductor, that is why you do not have p channel MESFETs. Now let us see if there are any other devices you are interested in.

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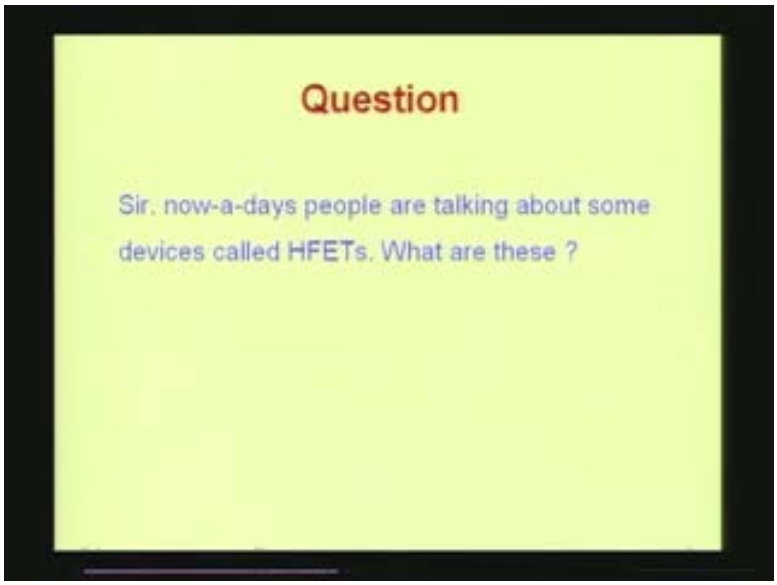

Sir, now-a-days people are talking about some devices called HFETs, what are these?
HFETs are Hetero Structure Field Effect Transistor. There are many other names of this device.

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For example, this device is also called Modulation Doped FET so MO D F E T that is MODFET. To understand why it is called so, let us look at this structure of the device. This device is made in compound semiconductors.

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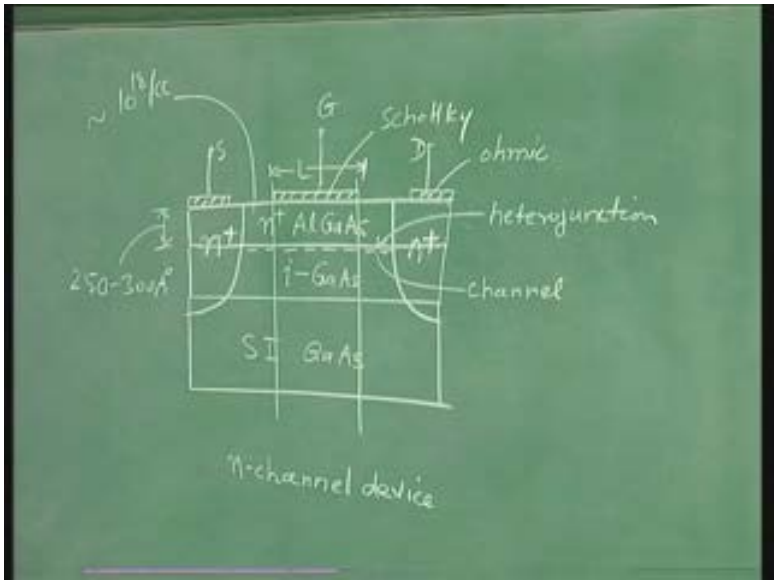

Let us start with a device that is made in gallium arsenide. Start with a semi insulating gallium arsenide. On this you grow an undoped high quality gallium arsenide. Further on this

you grow a heavily doped aluminium gallium arsenide layer n + aluminium gallium arsenide. So we are showing the structure for an n channel device. This is where you have the hetero junction, aluminium gallium arsenide, gallium arsenide. On the top of this you make a schottky contact this will constitute the gate and then you have the source and drain regions on which you have ohmic contacts. So this is the gate and this is a schottky type contact and this is ohmic contact. This is drain and this is source and this is the heavily doped region.

The channel here is formed by electrons at this hetero junction. These electrons are created by transfer from the heavily doped n-type aluminium gallium arsenide. So this is the channel, this is the hetero junction. This channel connects the drain and source and when you change the gate voltage this channel is modulated.

Now please note that if you want to modulate the channel you must apply a reverse bias to this gate so that a depletion region is created here that depletes this region fully and then it starts controlling the two DEG and it starts controlling the electrons. We will shortly see why it is called two DEG.

With reference to this structure let us understand why it is called a modulation doped Field Effect Transistor. What you are doing is, you are growing different layers on a substrate of various doping levels. So you grow one layer of one particular doping then you switch the dopend and grow another layer of a different doping. This process is called modulation doping.

In fact, the technology which has been responsible for realization of this device is MBE Molecular Beam Epitaxy which allows you to do such modulation doping with very thin precisely controlled layers and that is responsible for realization of this particular device. Here, for example; this layer which is very critical would be about 250 to 300 Angstroms and the channel length of this device which is this length here would be less than a micron even quarter micron. The doping in this n + region would be about 10 power 18 cc. Now, we have explained why it is called modulation dope FET. Let us look at some of the other names of this device which also has a relation to the operation. Selectively doped hetero junction transistor so S D H T that is the abbreviation.

‘Selective’ doping this particular phrase has the same meaning as modulation doping. These two names are more or less similar. Let us look at this name High Electron Mobility Transistor H E M T or HEMT. Why is it called a High Electron Mobility Transistor? What is happening here is that, a channel of electrons is in a very lightly doped or undoped semiconductor. That is why the mobility of these particular electrons is very high because there is no impurity scattering. When the doping in a semiconductor is low mobility of carriers is high because the impurity scattering is negligible. That is why it is called high electron mobility transistor. Let us look at another name for this device, that is, Two Dimensional Electron Gas FET or TEGFET.

What is this Two Dimensional Electron Gas?
This channel of electrons here is said to constitute a Two Dimensional Electron Gas or 2 – DEG.

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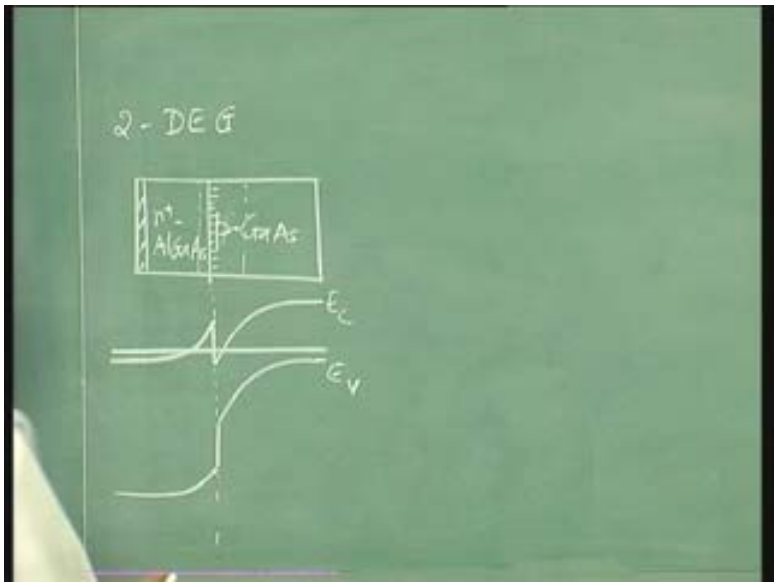

Let us understand why the electrons at the hetero junction constitute a Two Dimensional Electron Gas and what is a Two Dimensional Electron Gas?
Let us draw an energy band diagram of this particular hetero junction here. This is a wider band gap material as compared to this. Energy gap of AlGaAs is more than gallium arsenide.
So the energy band diagram would look something like this. We will turn this device 90° so that the gate is on the left hand side and junction is here.

We are drawing the energy band diagram of a structure like this so that we can relate it to other band diagrams which we have drawn. This is the schottky contact, this is the n + AlGaAs and this is the gallium arsenide. Now we are not interested in this band diagram at this particular contact but we are interested in this hetero junction, this is i gallium arsenide.
What is energy band diagram at this hetero junction?
This band diagram looks something like this.

This is AlGaAs and this is GaAs. This is the conduction band edge and this is the valance band edge. Your Fermi-level would be something like this. Now here it appears to be not really intrinsic but p-type, let us call it p gallium arsenide. It is basically lightly doped and it can be p-type or n-type it really does not matter but here in the band diagram it is p-type. This is the diagram drawn under equilibrium. All the electrons are here because they are transferred from the heavily doped aluminium gallium arsenide. The reason for this transfer is same as the reason for formation of the depletion width in this device. So whenever a junction is formed carriers will be transferred. Here what happens is that because the electron concentration is really high on this side when you draw the concentration diagram for this particular structure it would look something like this. Let me draw the diagram here.

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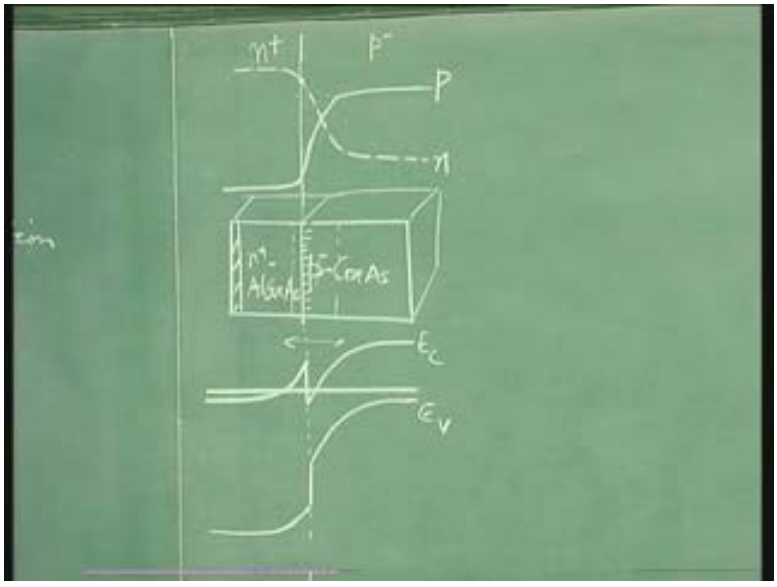

So this is the junction and if you draw the electron concentration it would look like this and hole concentration would look something like this. So this is p and this is n.

Let us show the n by a dotted or dashed line. Now what you find is, here the electron concentration at this point at the junction is much more than the hole concentration in the bulk so this region is inverted. This is an interesting PN junction and is called grossly asymmetric PN junction. It is asymmetric because doping is very high and it is n-type on this side and doping is very light and p-type on this side so it is grossly asymmetric in terms of doping. In such a case not only you have a depletion layer but you also have an inversion layer of electrons. If you draw this same diagram on linear scale you will see the inversion layer of electrons very easily because concentration of electrons at the junction is more than the hole concentration in the bulk.

Now these electrons if you see on the energy band diagram they are in a potential well here. This is the energy band diagram of the junction hetero junction; this is like a well this particular notch. So, electrons here cannot move in this direction.

Now, if you take the three dimensional picture it means they can only move perpendicular to this board along the cross sectional area of the junction, that is along this area. So they can only move along this particular cross sectional area. Therefore they can only move in a plane they cannot move this side because they are confined in this well and that is why it is called a Two Dimensional Electron Gas because they can only move in a plane or in two dimension and in the third dimension the motion is restricted. There are some advantages of this particular feature in the device. But those are beyond the scope of this particular course.

Here I only want to mention some aspects of the device, their operation and application. Now let us quickly see with the help of a few slides how this modulation doped FET can be developed from the devices that we already know.

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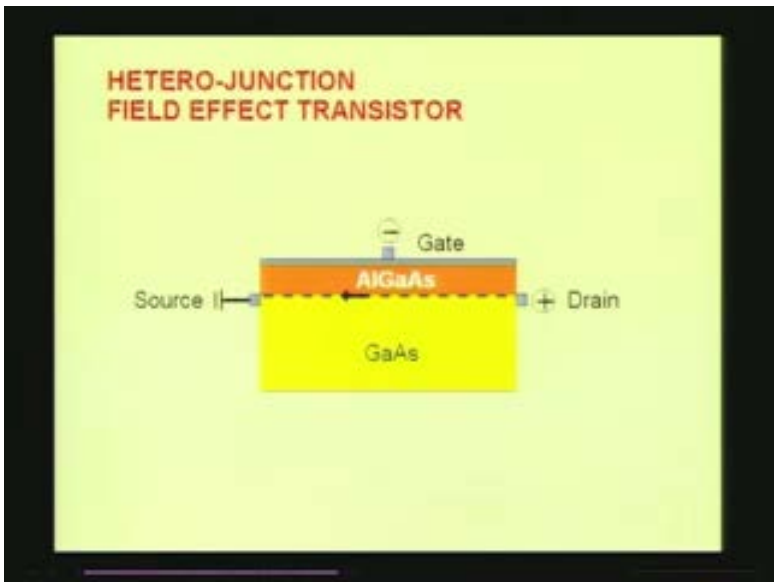

Here we have shown a simple conceptual diagram of an AlGaAs, GaAs, modulation doped FET or hetero junction FET or HFET. If you see this slide what we have shown there is, we have taken this device and we have simply taken this particular section for simplicity as we have been doing with other FETs and we are trying to explain how this particular simple structure works. Let us come back to the slide. You have to apply negative voltage to the gate to control the channel of electrons which is shown by a dashed line, the arrow here shows the direction of current when you apply drain to source voltage.

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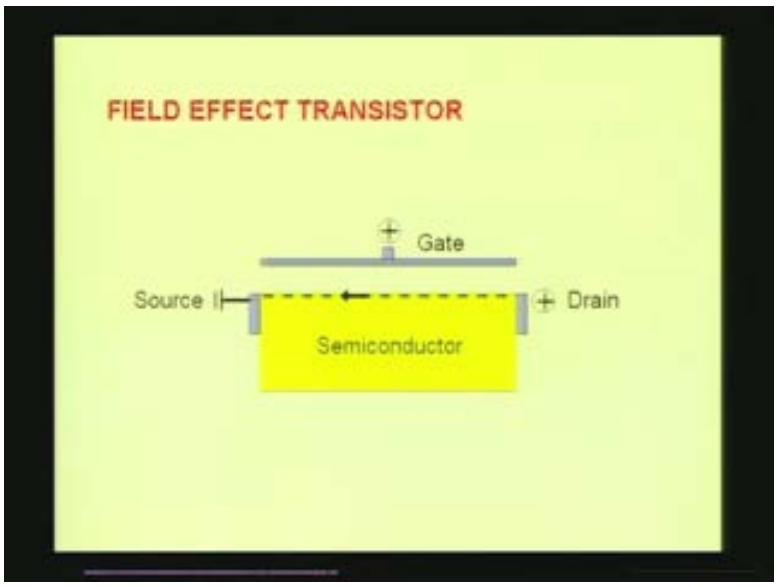

How can you develop this device from very simple principles?

Look at this structure which is a Field Effect Transistor. This is the basic idea proposed long ago in 1925 that how you can make a FET using a semiconductor. Now, when you apply gate, voltage electrons are attracted to the surface of the semiconductor and they will move from drain to source and this current is controlled by the gate, this is the basic idea of a FET.

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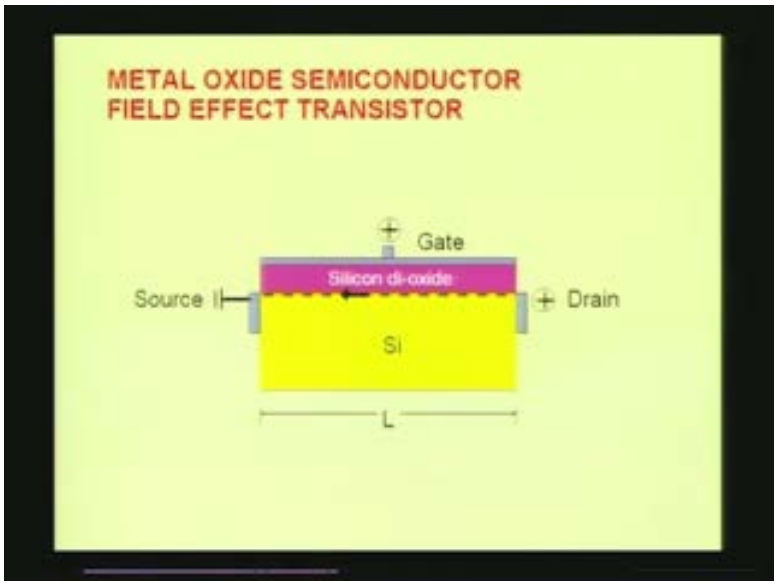

When you want to realize it in practise you introduce a silicon dioxide layer between gate and substrate. This device was originally made in silicon so this is the MOSFET Metal Oxide Semiconductor FET. Now let us see how you can modify this device progressively to get a HFET.

So first step is if you want to make the device in compound semiconductor to get the advantage of high mobility of electrons in gallium arsenide as compared to silicon is difficult because you do not have a very good insulator that you can deposit on gallium arsenide using a simple process.

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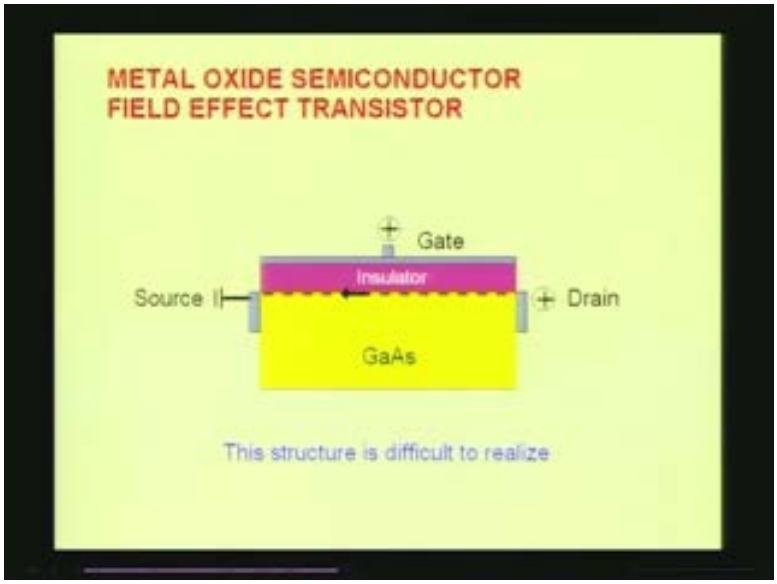

So on silicon the silicon dioxide can be deposited very easily by thermal oxidation but in gallium arsenide it is very difficult to get any oxide by a simple process and this is the problem. So, how do you rectify this problem?

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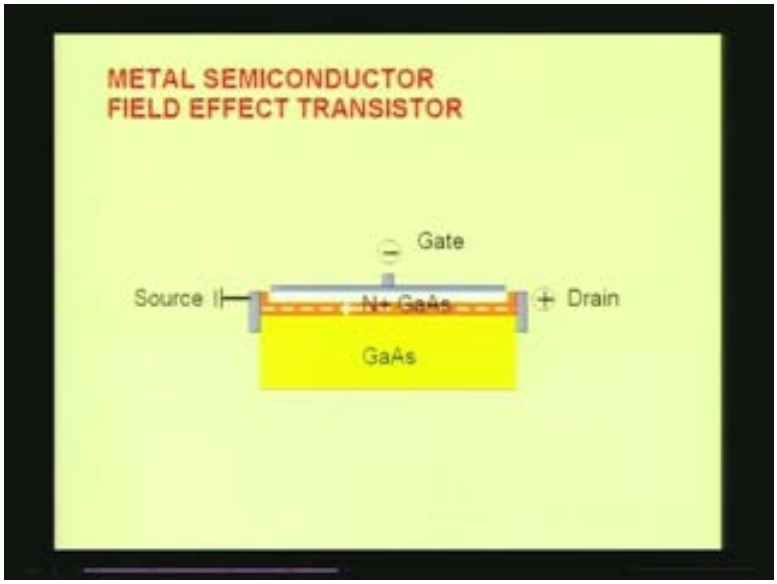

What you do is you push the gate down and have no insulator between the gate and substrate and instead you create a heavily doped layer of gallium arsenide which you can deplete using the gate. This is the concept of metal semiconductor Field Effect Transistor which we discussed just now. So, when you apply a negative voltage the doped region depletes as shown by the white region and you can have current flow from drain to source controlled by the gate by changing the depletion region.

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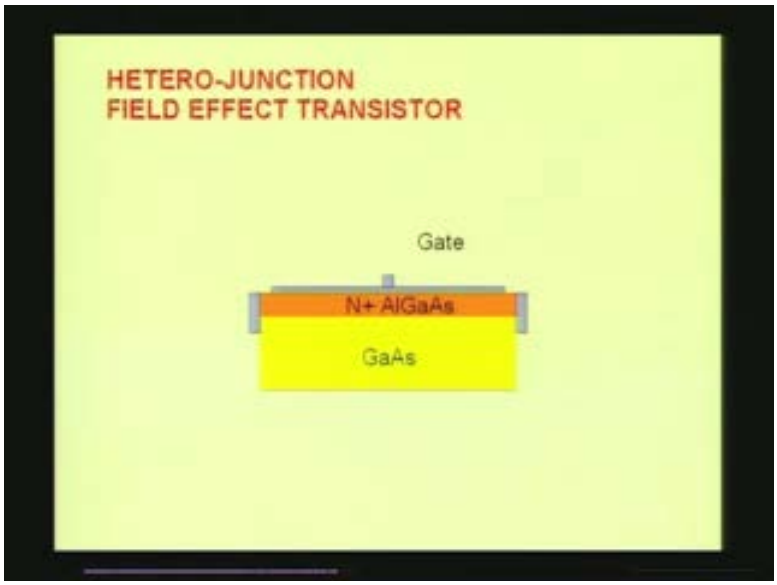

The next step is, you replace n + gallium arsenide by n + AlGaAs. Therefore now you have a hetero junction between the AlGaAs layer and the GaAs layer. That is the hetero junction Field Effect Transistor.

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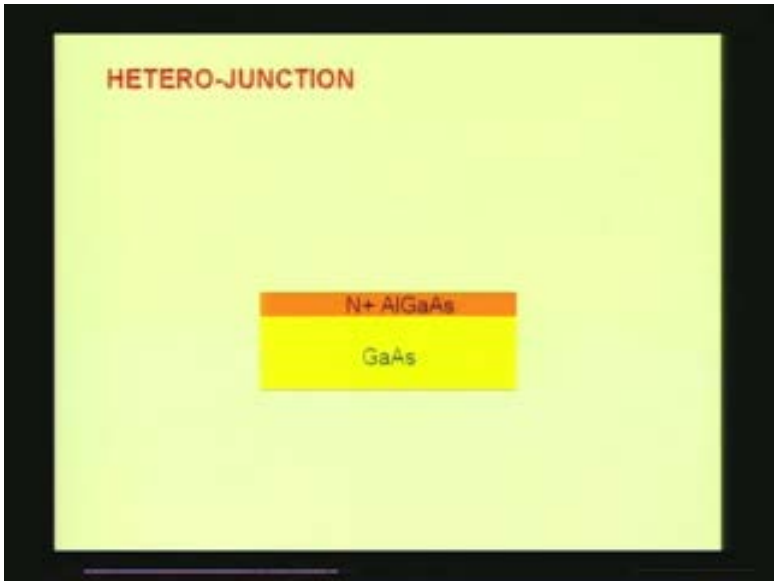

To understand this you must understand the hetero junction. So, as we have explained, in a hetero junction you have a large concentration of electrons at the junction.

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How do you get that? Start with a n + gallium arsenide gallium arsenide which is a homo-junction. This is asymmetric or rather grossly asymmetric homo-junction because heavily doped gallium arsenide is in contact with a very lightly doped gallium arsenide.

So this is called grossly asymmetric because doping levels are very different on either side and they are of opposite polarity. In this case electrons are created at the junction as we have explained using this concentration diagram here.

Look at this diagram which we have done for a simple PN junction which is not grossly asymmetric. Here it is shown for a grossly asymmetric junction. Using this concentration we explained the creation of these electrons here. Now, when you want to enhance this electron concentration you put a wide band gap material instead of the n + gallium arsenide.

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Now here you have asymmetric or a grossly asymmetric junction as far as doping is concerned and in addition you have a hetero-junction because the AlGaAs layer has a different energy gap and other parameters than the gallium arsenide layer. So, as a result of this because the AlGaAs layer has a wider gap than gallium arsenide the electron transfer is enhanced as it is shown here. Therefore, as compared to gallium arsenide where you have small number of electrons or gallium arsenide homo-junction where you have small number of electrons in a hetero-junction the electron concentration is raised because of the energy gap difference.

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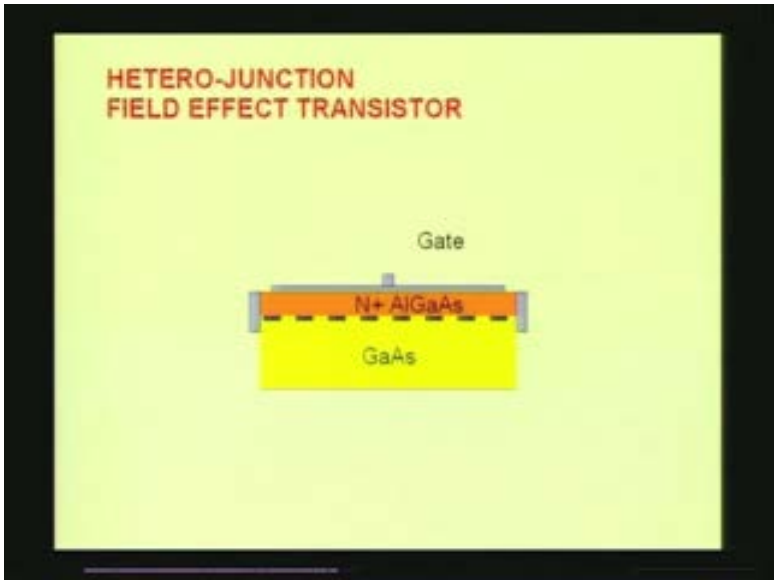

Now you make a device using this particular hetero-junction. You put a gate, source and drain.

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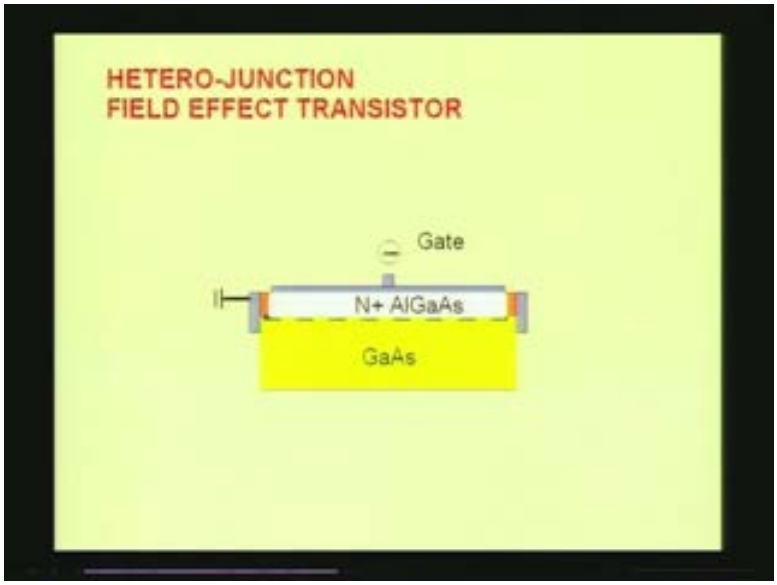

And then when you apply a negative voltage to the gate and if the gate voltage is sufficient to deplete the entire n + region and reach the electrons then the depletion region can deplete the electrons also as shown here. So, you can see that when you apply a voltage the depletion is reaching the electrons and it is depleting them.

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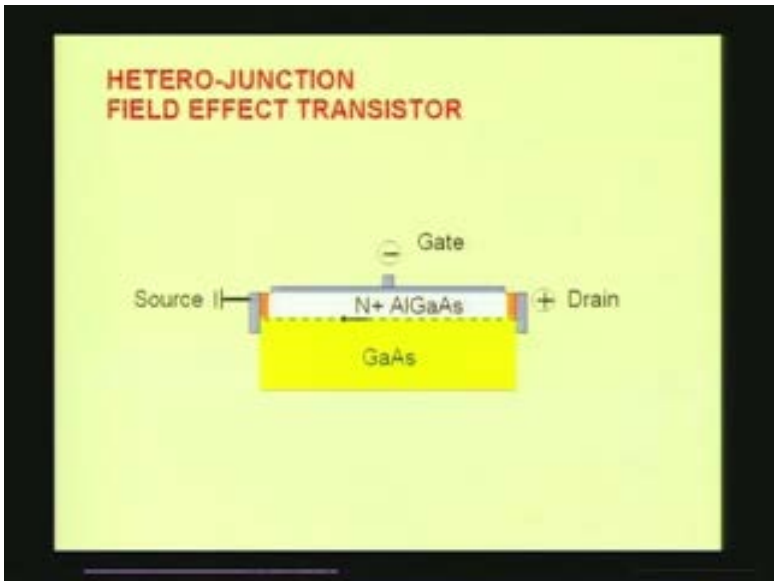

Now you have a current between drain and source that can be controlled by the depletion layer or the gate voltage. So, that is the idea here of a hetero-junction Field Effect Transistor.

What are the advantages?

As compared to MESFET the mobility is much higher. That is the main advantage here because the electrons are in a lightly doped region. In a MESFET the electrons are moving in a heavily doped region whereas in a HEMT the electrons are moving in a lightly doped region since their mobility is high. There are other advantages also but because of this the HEMT or the HFET can operate at much higher frequencies than MESFET. Now let us see the other devices of interest to you.

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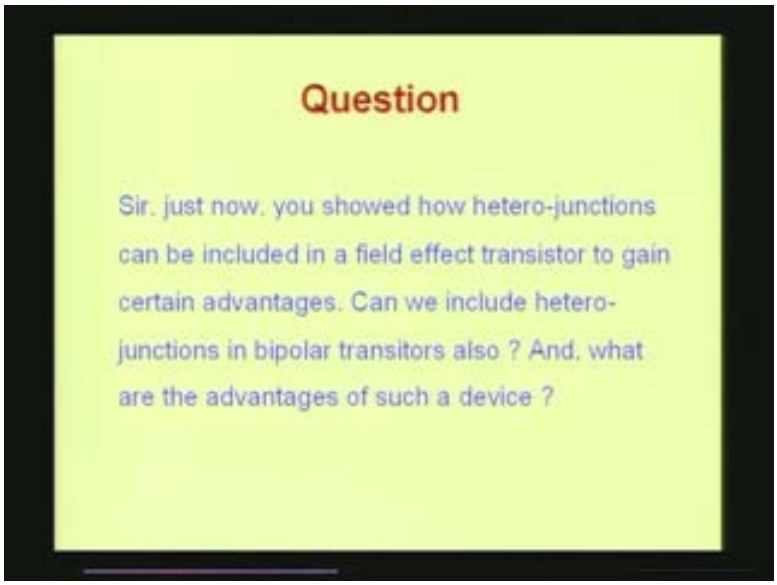

Sir, just now you showed how hetero-junctions can be included in a Field Effect Transistor to gain certain advantages. [43:02] Can we include hetero-junctions in a bipolar transistor also? And what are the advantages of such a device?

Yes, we can include hetero-junctions in bipolar transistor also and such a device is called hetero-junction bipolar transistor. Let us what are the advantages of the hetero-junction and where it is included in a bipolar transistor, this is the structure of a BJT.

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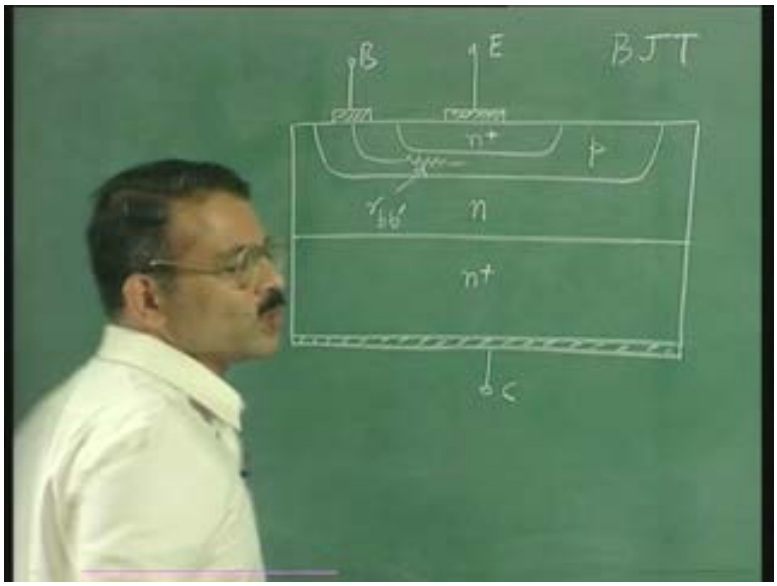

Now, you know that the modern BJT the beta depends on injection efficiency. That is, in terms of this diagram if you see here the flow diagram is shown for NPN transistor. Most of the electrons which are injected from emitter to base are transferred to collector.

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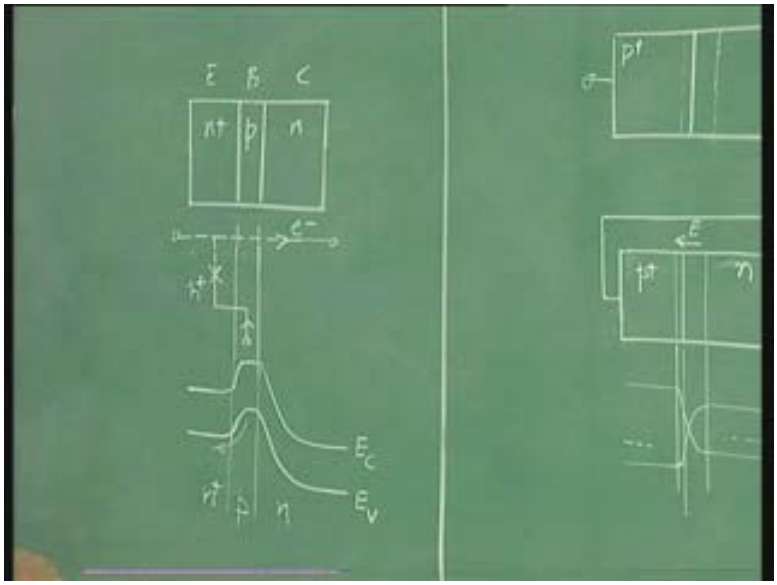

But the beta is not very high because there is this hole current injected from base into emitter and this is what is responsible for the non unity injection efficiency. So, if you can cut down this hole current then your beta will be increased tremendously.

How to cut down this hole current?

Let us look at the energy band diagram here. This barrier height here associated with the valance band decides how much hole current is injected. So, if you can increase this barrier height for movement of holes from p region to n region then less hole current will be injected, here this is p and this is n. So a simple way of increasing the barrier height is to introduce a hetero-junction here so make the n + region in a semiconductor of higher band gap than the p region. If you do that this is what will happen.

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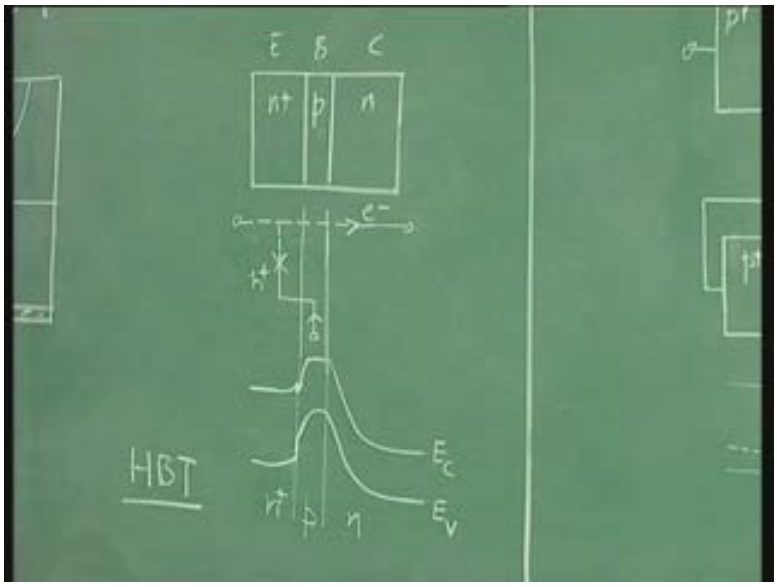

Here the energy band diagram will look as something like this so that this particular jump in the valance band edge gives rise to a greater barrier height here and cuts down this hole current. Of course it will also alter the band diagram of the device here in the conduction band. So here in fact you may find that you have something like a notch but we are not going to discuss the effects of these. Mainly it is the effect of this that is responsible for cutting down the hole current. Now there are other related advantages when you make this modification. The advantages are that now you can decrease the doping of the emitter once you have this method of increasing the barrier height.

Mainly you put heavy doping in the emitter so that you get a higher barrier height and you cut down the hole injection. Now since this barrier height advantage is being gained from hetero-junction you do not raise the doping very much but you can cut down the doping in the emitter. When you cut down the doping in the emitter what happens is the emitter depletion width expands so the emitter capacitance is decrease. Therefore again this is very nice for high frequency operation.

Similarly, you can rise the doping in the base. That is, the asymmetry of the doping between the emitter and base can be reduced once you introduce the hetero–junction. So, what are the advantages if you increase the doping in the base?

The increase in the doping in the base cuts down this particular rbb' the base spreading resistance.

As you have seen in the equivalent circuit of the bipolar transistor at high frequencies the rbb' is responsible for fall in the frequency response or performance at high frequencies. So, increasing the doping in the base enables you to cut down rbb'. So cutting down rbb' and cutting down the emitter capacitance because of lowering of the doping in the emitter the device can now be operated at high frequency. That is why HBT that we are talking about here can be operated at high frequencies and has a very high beta.

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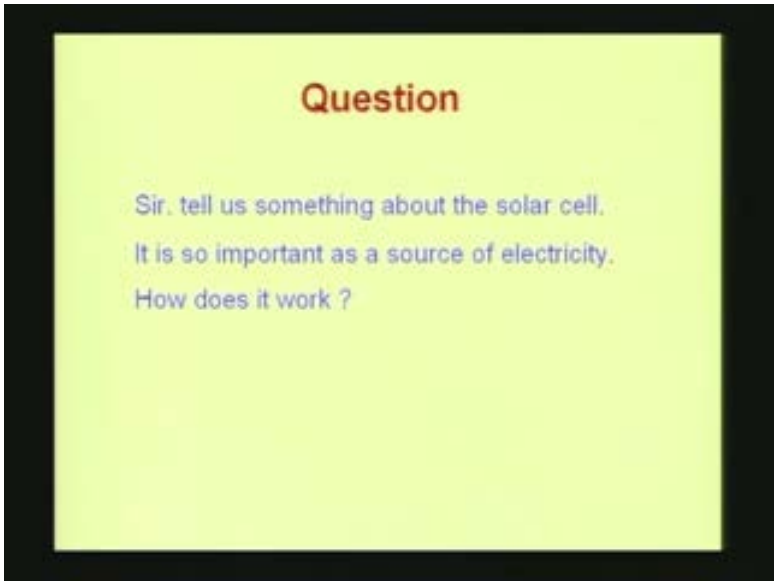

Sir, tell us something about the solar cell. It is very important as a source of electricity. How does it work?

The solar cell's working is very simple once you understand the PN junction. Let us look at this PN junction.

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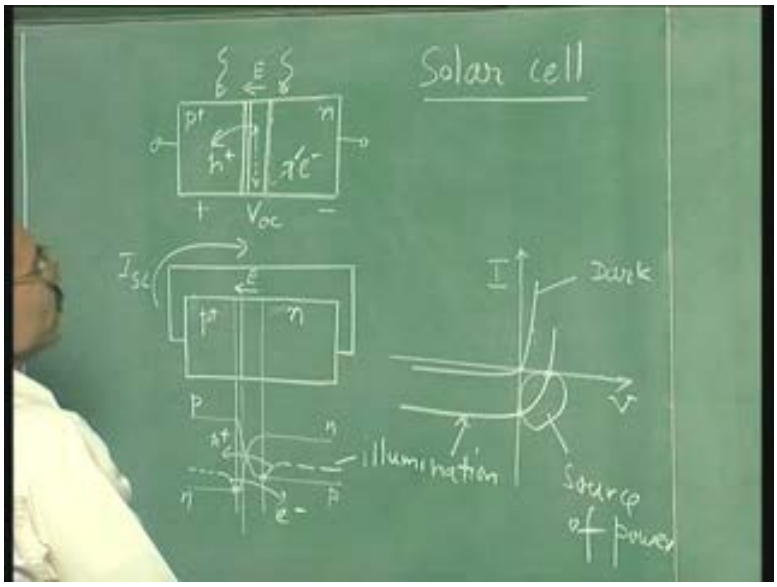

Now, in the absence of light these are the current voltage characteristics. Let us see what happens when you shine light. This light generates electron hole pairs throughout the volume. Let us assume this, actually this is not true. We will see what happens in practise. But for simplicity to understand the operation let us assume uniform generation of electron hole pair throughout the volume because of light.

Now what would happen here?
If this is open circuited you have a built in voltage from n region to p region here, an electric field directed like this. The holes generated within depletion layer will move to the p side and electrons generated here will move to the n side. So there is a separation of electrons and holes because of this built in electric field, the generated electrons and holes.

Since the holes move to the p side and electrons to the n side they will all get piled up here but they cannot move out because this is open circuit. So obviously the device will become positive on the p side and negative on n side. There will be a slight shrinking of the depletion region because of this forward bias. So you are able to measure a voltage between these two terminals created by separation of generated electron hole pairs.

Once electron hole pairs generated, let us say these are electrons and these are the holes so holes move this side and electrons are moving this side so that is how this is created. So on

the I V characteristics here once you shine light this point will move to the right and when there is no current you have a positive voltage. Let us see what happens if you short the device.

If you short the device the concentrations look like this under equilibrium conditions. Now you are shining light so electron hole pairs are increased. So here this is hole concentration and this is electron concentration. So, minority carriers are raised up as shown by the dotted line. We are not showing any change in majority carriers because this is a log scale. Now what happens at the junction is because this is shorted the concentration of minority carriers at the junction cannot change by Boltzmann relation. Therefore, your excess hole concentration which is high in the bulk should fall. The excess minority carrier concentration should fall as it nears the junction and it should become equal to the equilibrium concentration. So this is the kind of concentration diagram you will have under illumination.

As a result of this you have holes moving this side and electrons here diffusing this side.

Now these holes will move out and these electrons will move out of this so as a result there will be a current in this direction. This is the so-called short circuit current, like the voltage here in open circuit conditions is called open circuit voltage this is called short circuit current because this is shorted and you have a current. So, on this diagram you will find this point will move down, the current for $V = 0$ is non zero and it has some value dependent on the extent of intensity of light. So your characteristics under illuminated conditions would be something like this. So in this region here the device is behaving like a source of power.

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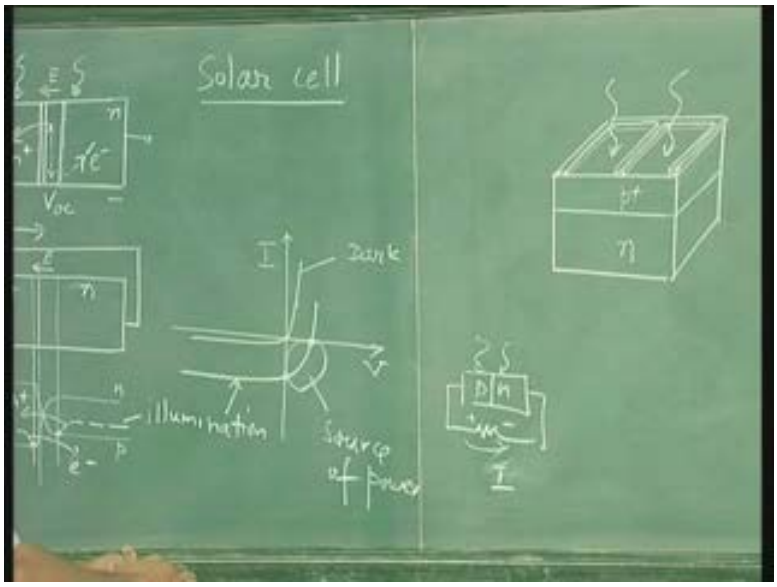

So if you connect a resistor to this device like this you will have a current flowing into this and you will have a voltage drop so when you shine light this happens. Therefore this is how a diode acts like a source of power.

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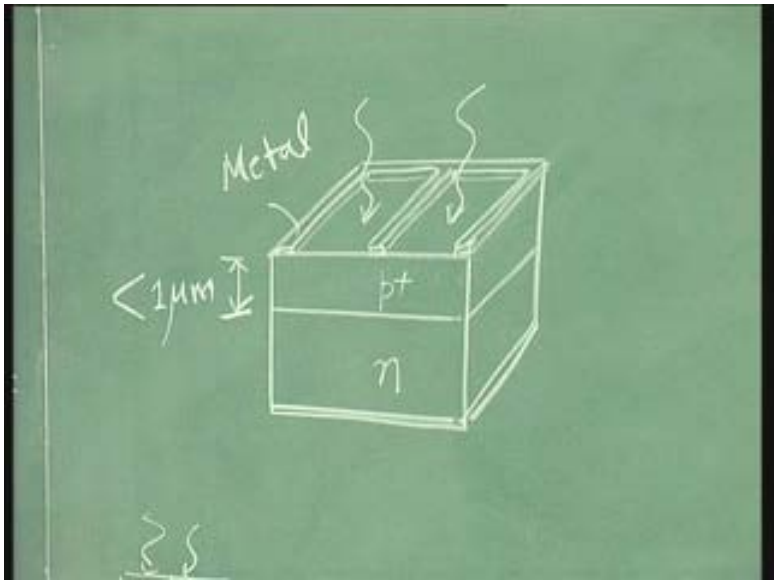

Now, this is a construction of the solar cell in practise. When you shine light the light should be absorbed by the semiconductor otherwise no electron hole pairs will be generated. The

metal contact here is made very and large regions of semiconductor are left open to light. This is the metal contact on the top and similarly you have a contact at the bottom. Further this junction should be very close to the interface because the light is absorbed in a very small region of about a micron or so. This is in fact less than a micron in a solar cell. So it is necessary to make it as shallow as possible. In fact it is made up to about 0.2 microns or even lower. That is the construction of the solar cell.

Now we have seen a number of devices in this particular lecture. What we will do in the remaining few minutes is to give a very brief summary of the entire course.

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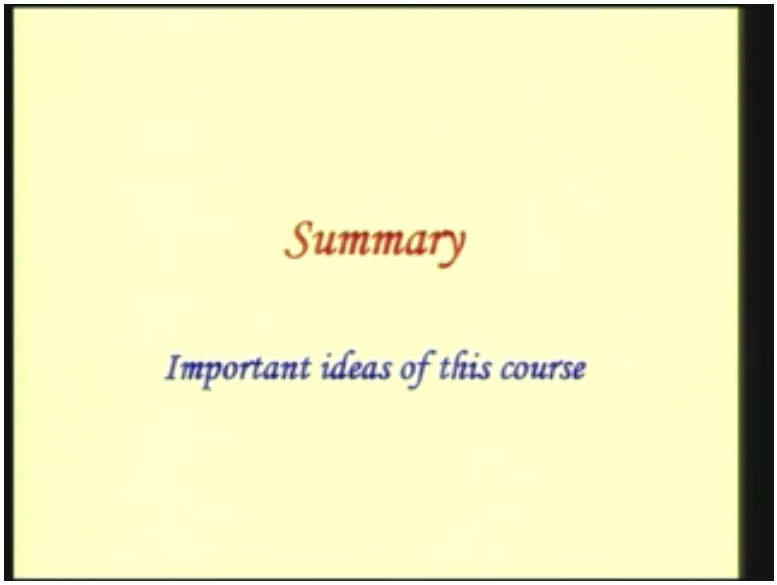

Important ideas of this course: What are they?

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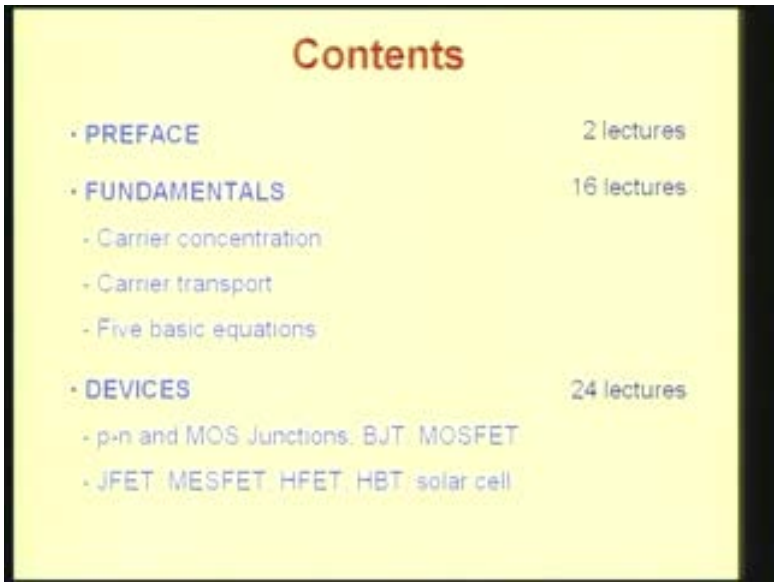

We can divide the course into three parts. There are 2 lectures of preface, 16 lectures of fundamentals covering concentration and transport of carriers and the five basic equations and 24 lectures of devices where in we discussed the p n and MOS junctions, BJT and the MOSFET and very briefly we also discussed the JFET MESFET HFET HBT and solar cell.

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Let us look at the preface.

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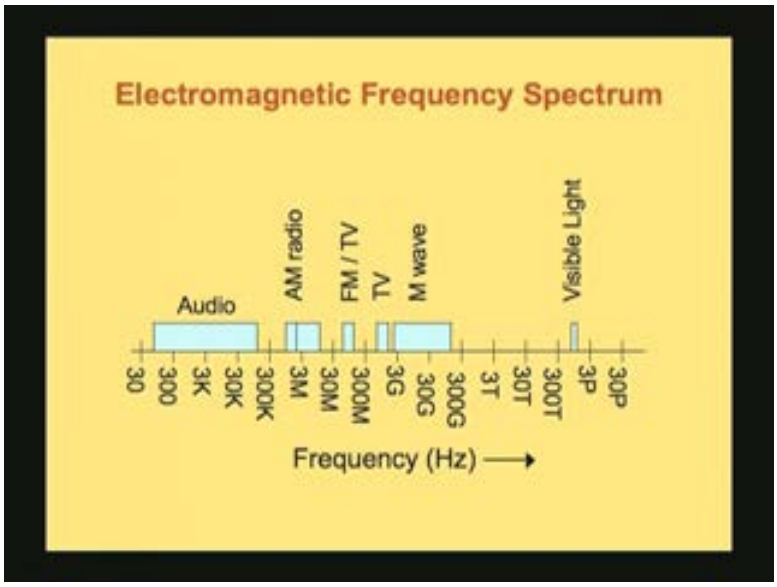

Here we discussed the classification of devices into low frequency and high frequency devices. We looked at the frequency spectrum. The regions in this spectrum were devices that are required. We also classified the devices into power and small signal devices.

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Then we discussed the uniqueness of semiconductor technology. The fact is that this technology requires a large capital investment because the processing conditions are very

stringent. So you need an ultra clean room and you need a single crystal material. The products of this technology however are very easy to use. We also saw how inventors, scientists and engineers have contributed to the evolution of this technology.

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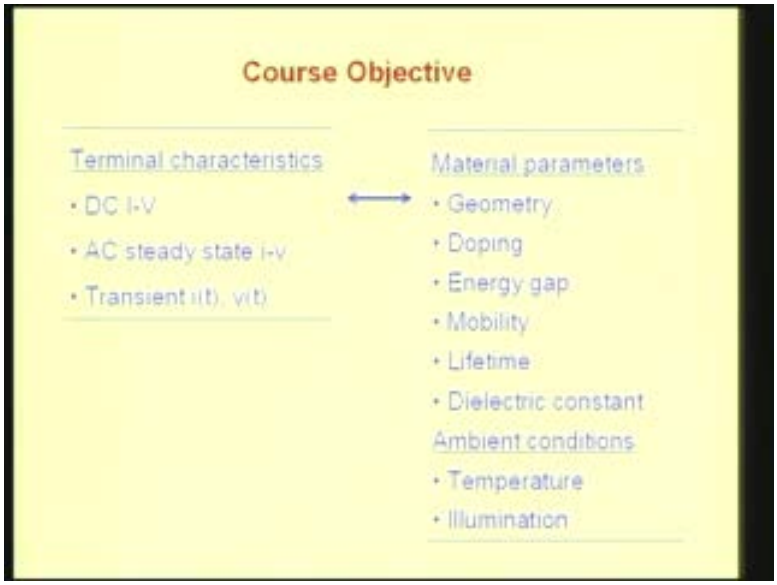

Then, we discussed the course objectives where in we said we want to relate the terminal characteristics to material parameters and ambient conditions. The terminal characteristics we discussed were the DC I-V and the AC steady state i-v or the small signal characteristics. We did not discuss the transient characteristics although these are also important. The material parameters are geometry, doping, energy gap, mobility, lifetime and dielectric constant and the ambient conditions are temperature and illumination.

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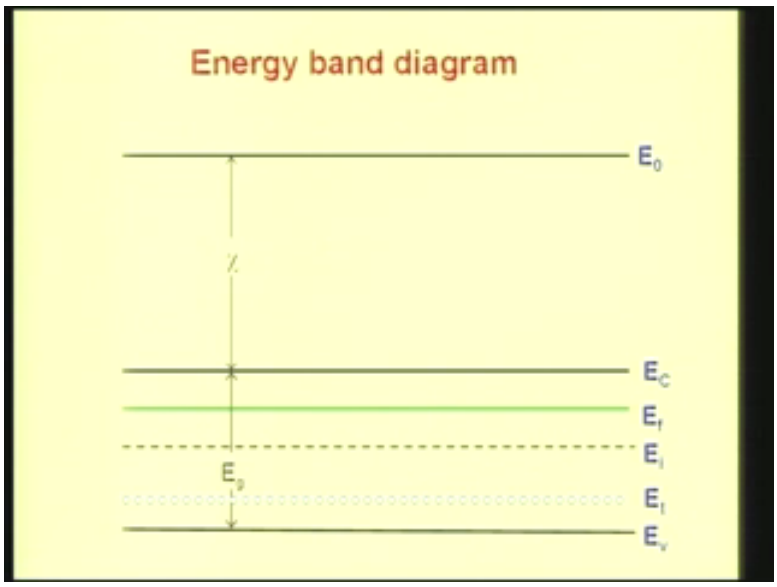

The fundamentals in detail:

We discussed the energy band diagram namely the vacuum level E0, the conduction band edge Ec, the Fermi-level Ef, the intrinsic level EI, the impurity level E suffix I and the valance band edge Ev. We also mentioned the difference between E0 and Ec as electron affinity kai and the difference between Ec and Ev as the energy gap.

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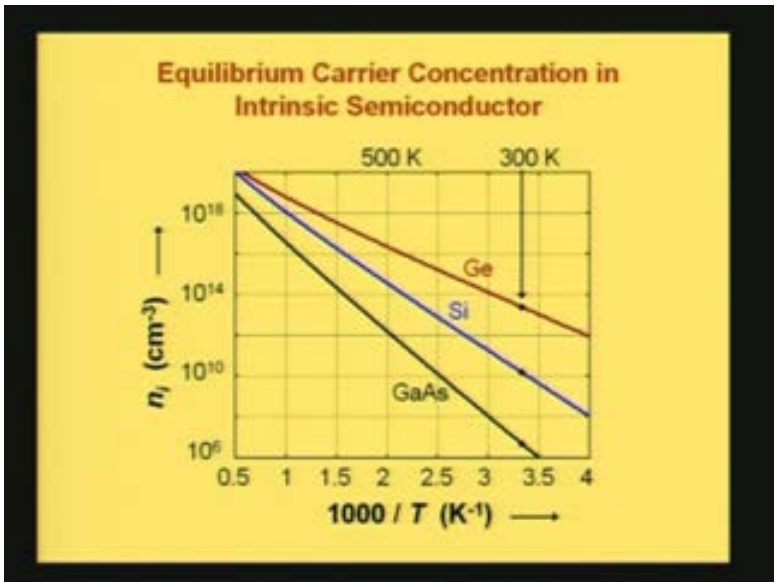

Then we saw the equilibrium carrier concentration in an intrinsic semiconductor as to how it varies exponentially with temperature and energy gap.

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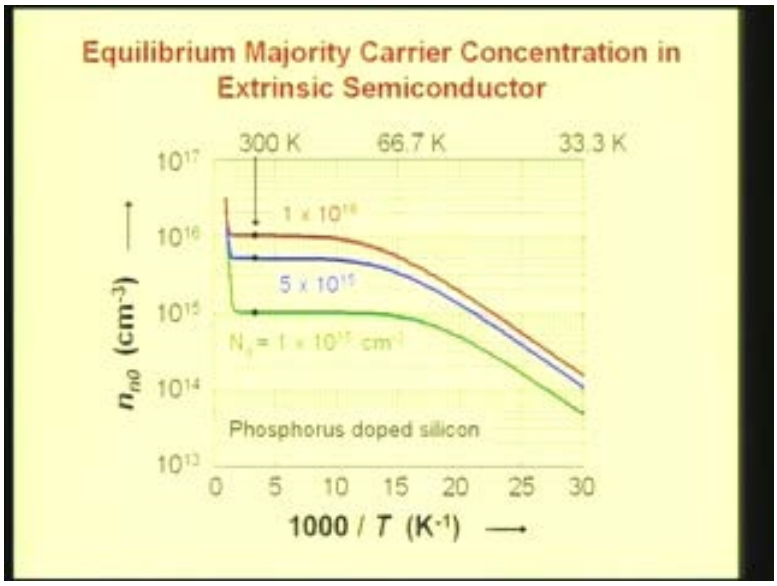

Then we discussed the equilibrium majority carrier concentration in an extrinsic semiconductor as how it varies with temperature and doping.

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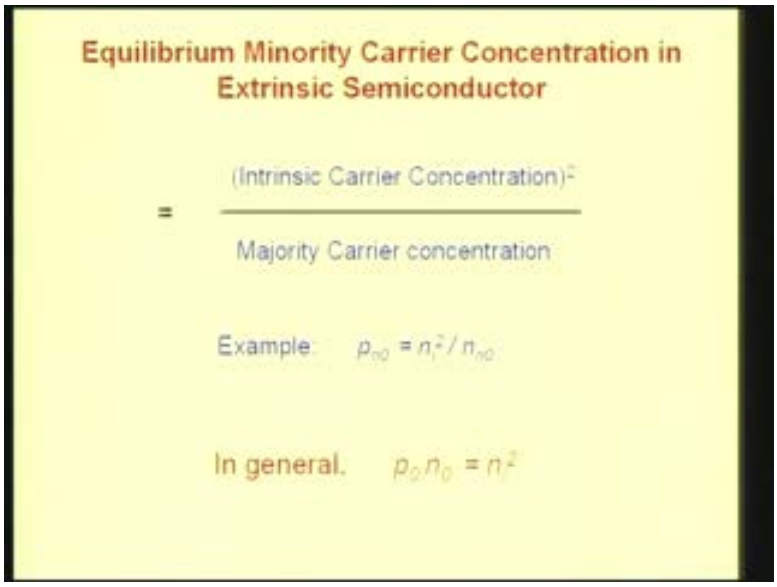

Then we said that the minority carrier concentration at equilibrium is obtained as intrinsic carrier concentration square divided by majority carrier concentration because p0 × n0 under equilibrium is ni^2.

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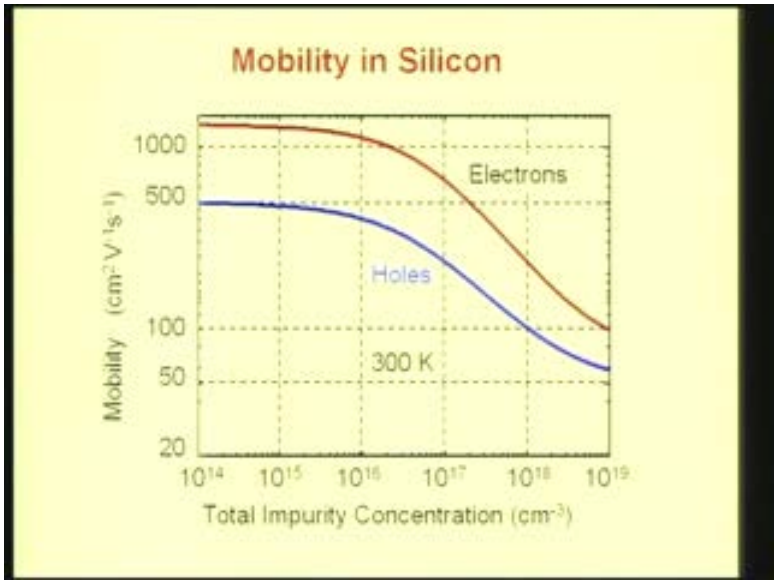

We also saw how the mobility varies with impurity concentration and how it is different for electrons and holes.

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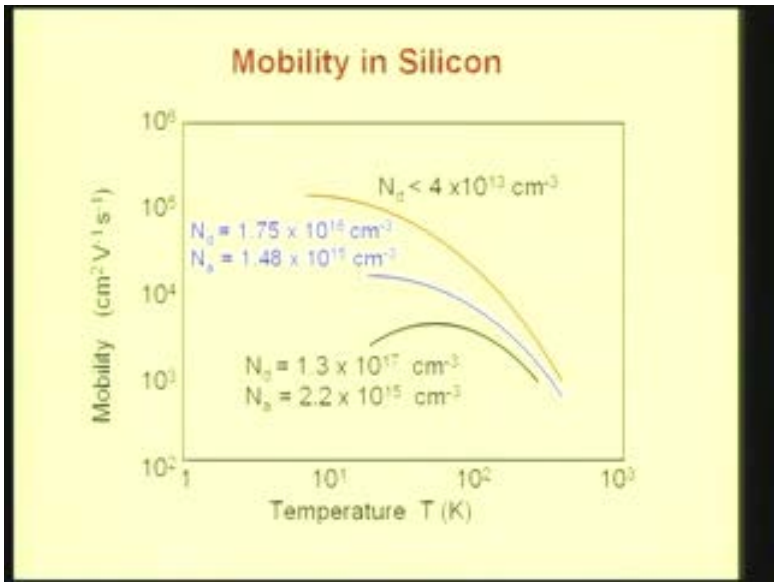

We also saw how the mobility varies with temperature.

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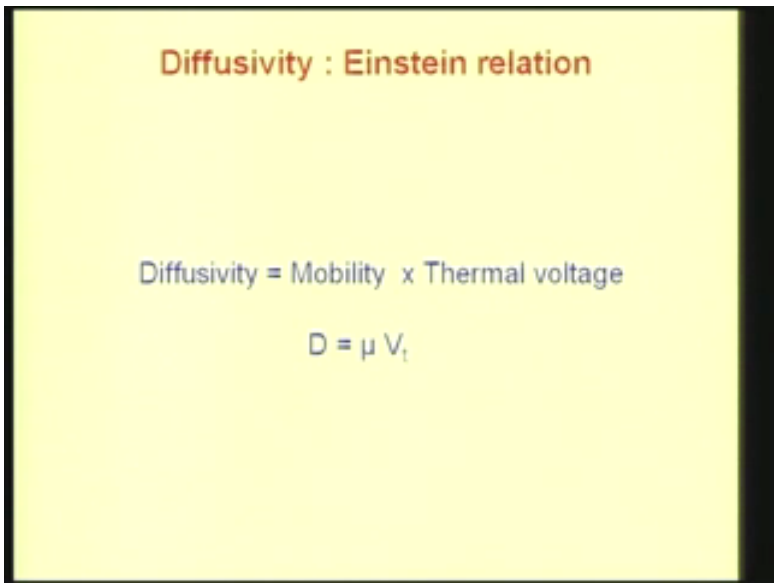

We said that the diffusivity is obtained from the mobility using the Einstein relation. It says D = mu × Vt which is the thermal voltage.

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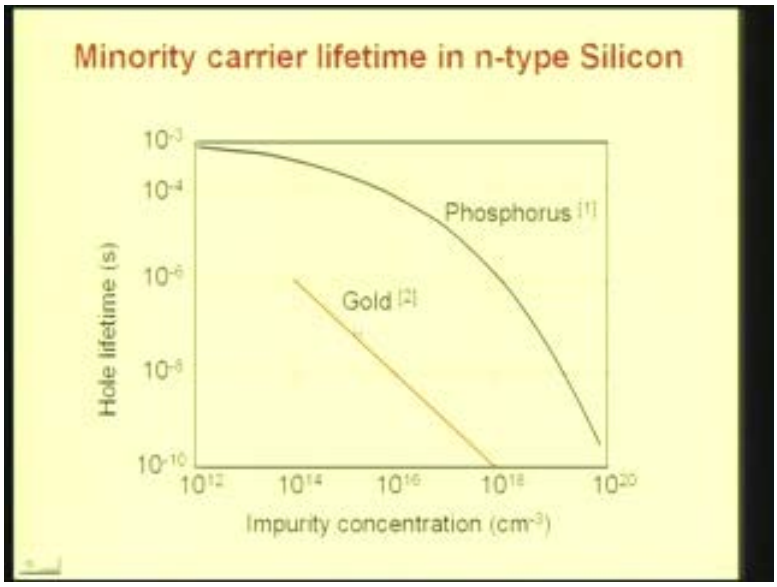

Then we discussed the carrier lifetime which characterises the decay of excess carriers. There are two types of lifetimes where one is associated with the direct recombination and the other associated with the indirect recombination. In indirect band gap semiconductors it is this indirect recombination that is predominantly responsible for excess carrier decay.

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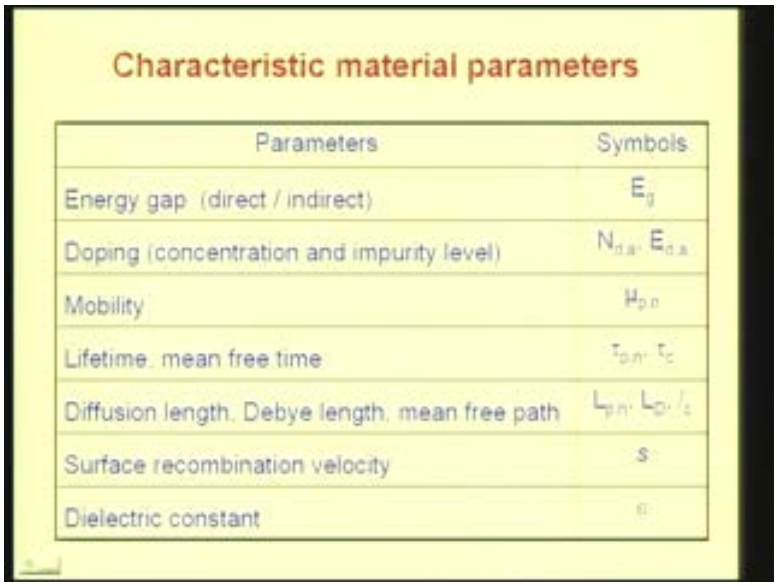

Summarize the characteristic material parameters. Energy gap, doping, mobility, lifetime, mean free time, diffusion length, Debye length, mean free path, surface recombination velocity and dielectric constant.

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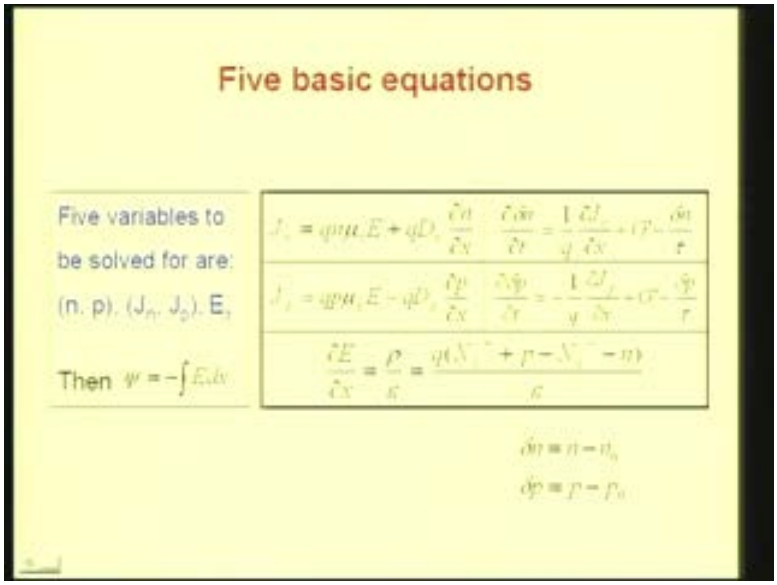

Then we saw the five basic equations. These were the transport and continuity equation for electrons, the transport and continuity equation for holes and the continuity equation for electric flux or the Gauss law. The five basic variables to be solved for are n p, J n J p that is the two current densities for electrons and holes and the electric field E.

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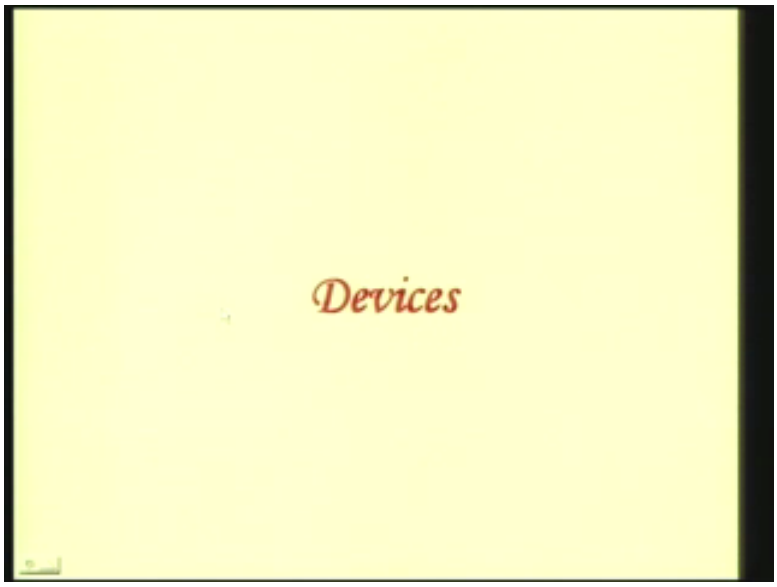

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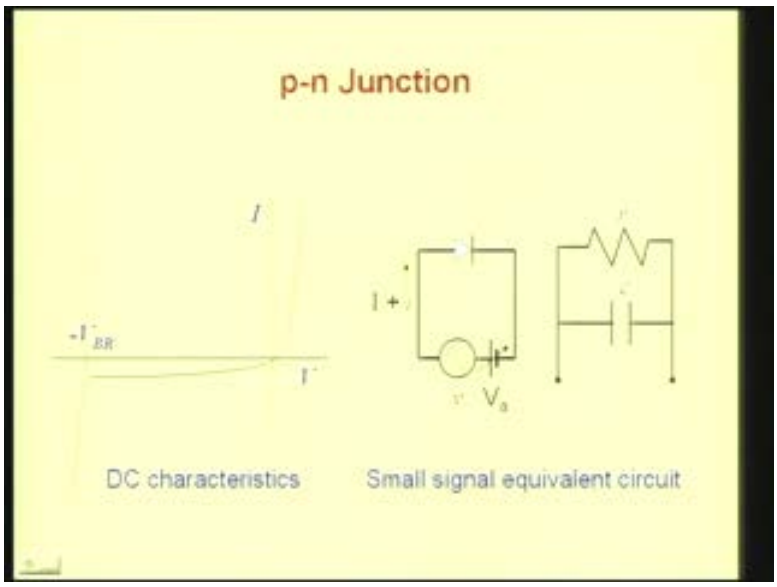

Then we looked at the devices. We saw the DC characteristics of p-n junctions and derived an equation for this. And we also saw the small signal equivalent circuit which talks about how the small signal current varies with small signal voltage when these small signal conditions are superimposed over DC.

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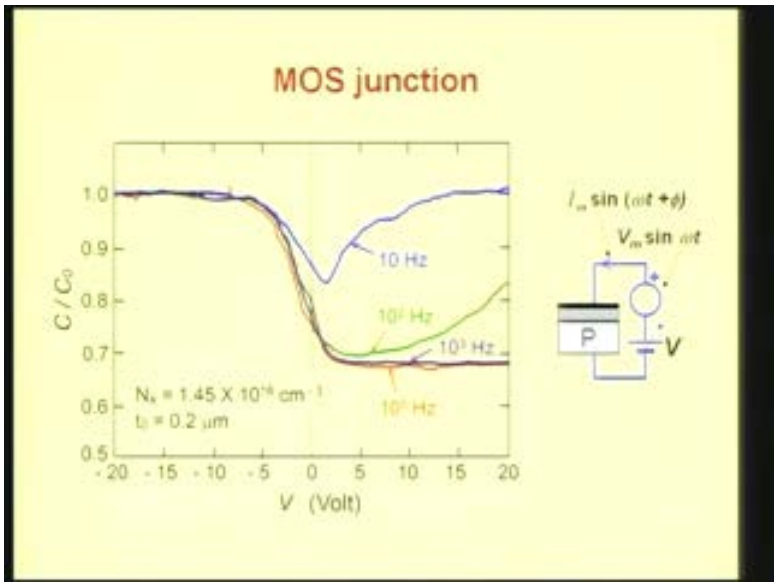

We saw the capacitance voltage characteristics of the MOS junction. The MOS junction does not have any DC current voltage characteristics.

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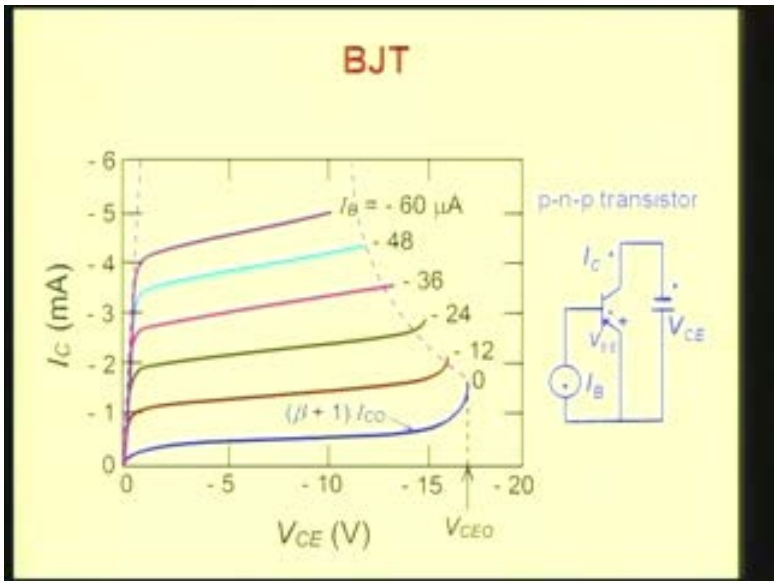

Then we saw the DC current voltage characteristics of the Bipolar Junction Transistor as to how the collector current varies with collector emitter voltage as base current is varied.

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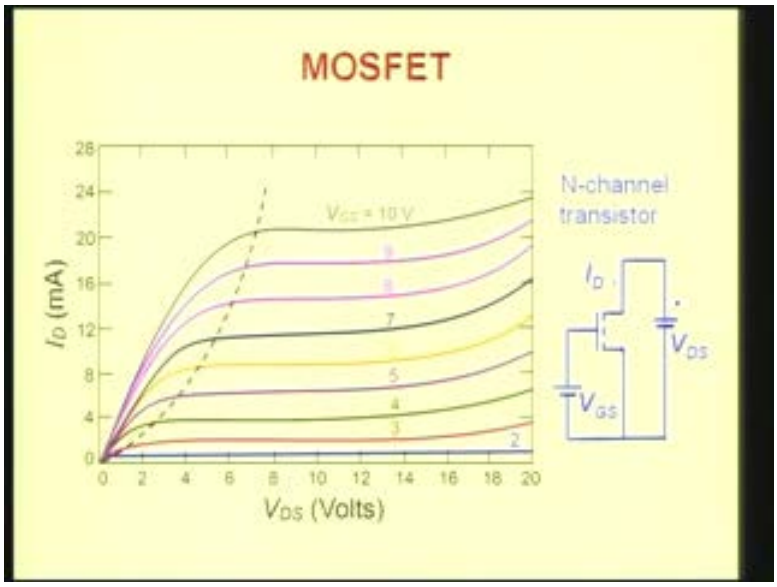

We saw the similar characteristics for MOSFET as how the drain current varies with drain source voltage when the gate source voltage is varied. The MOSFET is a voltage controlled device while the BJT can be regarded either as a current controlled or a voltage controlled device.

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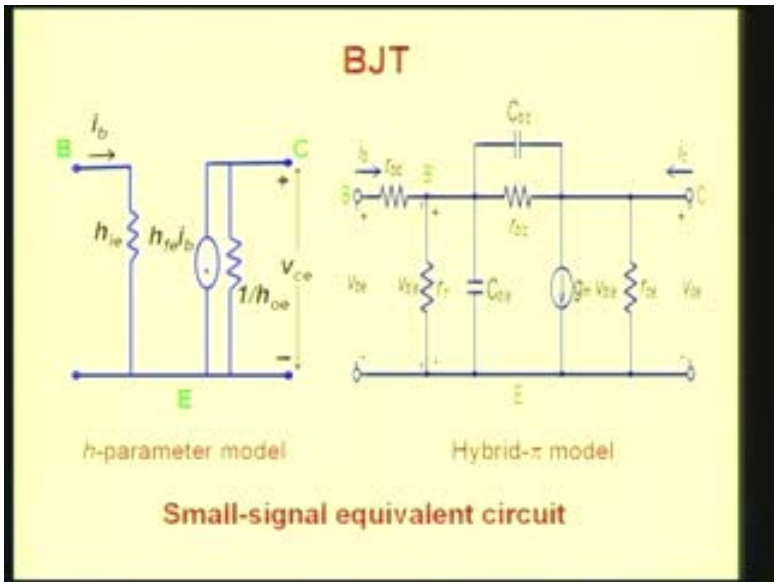

Then we saw the small signal equivalent circuit of the BJT. The low frequency equivalent based on the h parameter model and the hybrid pi equivalent circuit which is applicable at high frequencies.

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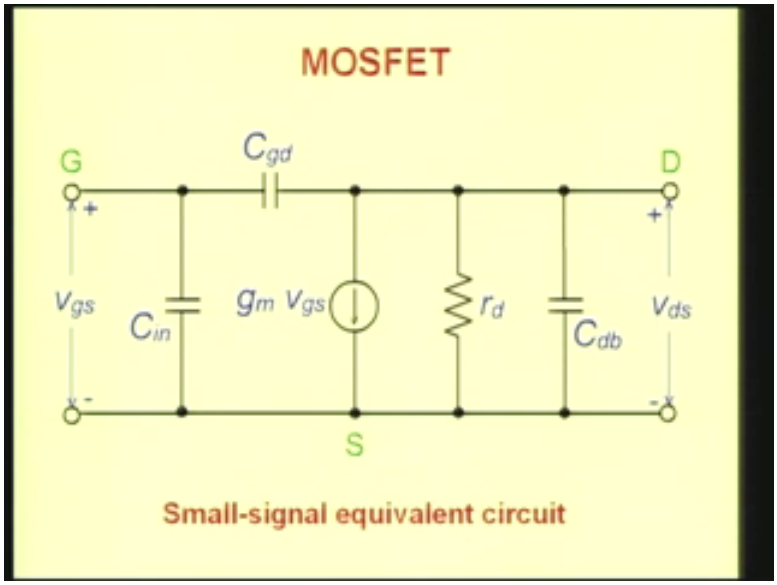

The MOSFET small signal equivalent circuit looks very much like the BJT equivalent circuit where in you have a pi like arrangement of varies components.

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And with that we came to the end of the course. So, thank you for sitting through 42 lectures of this course. I hope these lectures have aroused your curiosity in the field of semiconductor devices and you have developed an interest in knowing more about them and hopefully some of you will think of pursuing research in this area.